<u>Amendments to the Claims</u>

1. (Currently Amended) A power efficiency control (PEC) circuit comprising a plurality of multiplexers (MUXs) having a common input node (IN) <u>for receiving a single input signal for driving both the UOP and LOP</u>, an upper output node (UOP) and a lower output node (LOP), wherein the plurality of MUXs are configured to generate output signals at UOP and LOP in response to only [[an]] <u>the</u> input signal at IN such that during an input signal transition at IN, a control electrode for the UOP and the LOP are driven towards opposite voltage supplies so that the UOP and the LOP are never on simultaneously.

2. (Currently Amended) A power efficiency control (PEC) circuit comprising a plurality of multiplexers (MUXs) having a common input node (IN) <u>for receiving a single input signal for driving both the UOP and LOP</u>, an upper output node (UOP) and a lower output node (LOP), wherein the plurality of MUXs are configured to generate output signals at UOP and LOP in response to only [[an]] <u>the</u> input signal at IN such that during an input signal transition at IN, the UOP and the LOP are never on simultaneously, wherein the plurality of MUXs is configured to put the UOP and LOP simultaneously in a tri-state condition solely during the input signal transition.

3. (Previously Presented) The PEC circuit according to claim 2, wherein the output signals at UOP and LOP are CMOS compatible output pre-driver signals.

4. (Previously Presented) The PEC circuit according to claim 2, wherein the plurality of MUXs are further configured as a pre-driver stage comprising a CMOS UOP pre-driver and a CMOS LOP pre-driver.

5.(Previously Presented) The PEC circuit according to claim 4, wherein the CMOS UOP pre-driver comprises a MUX to control a PMOS transistor in the UOP and the CMOS LOP pre-driver comprises an MUX to control a NMOS transistor in the LOP.

6. (Previously Presented) The PEC circuit according to claim 2, wherein the plurality of MUXs are further configured such that during an input signal transition at IN, the output signal at UOP and the output signal at LOP reach their final states at different points in time.

7. (Currently Amended) A power efficiency control (PEC) circuit comprising:

an upper output node (UOP);

a lower output node (LOP);

a common input node (IN) <u>for receiving a single input signal for driving both the UOP and LOP</u> ; and

means for controlling the UOP and LOP in response only to [[an]] <u>the</u> input signal such that during a transition of the input signal at IN, a control electrode for the UOP and the LOP are driven toward opposite voltage supplies so that the UOP and the LOP are never on simultaneously.

8. (Previously Presented) The PEC circuit according to claim 10, wherein the means for controlling the UOP and LOP comprises a CMOS UOP pre-driver stage and a CMOS LOP pre-driver stage.

9. (Previously Presented) The PEC circuit according to claim 8, wherein the CMOS UOP pre-driver stage comprises a multiplexer to control a PMOS transistor in the UOP and the CMOS LOP pre-driver stage comprises a multiplexer to control a NMOS transistor in the LOP.

10. (Currently Amended) A power efficiency control (PEC) circuit comprising:

an upper output node (UOP);

a lower output node (LOP);

a common input node (IN) <u>for receiving a single input signal for driving both the UOP and LOP</u>; and

means for controlling the UOP and LOP in response only to [[an]] <u>the</u> input signal such that during a transition of the input signal at IN, the UOP and the LOP are never on simultaneously, wherein the means for controlling the UOP and LOP is operational to configure both the UOP and LOP to be in a tri-state condition solely during the input signal transition.

11. (Currently Amended) A method of controlling a CMOS buffer having pull-up and pull-down circuitry, the method comprising the steps of:

providing a multiplexer pre-driver configured to generate a PMOS output signal and an NMOS output signal in response to only ~~an input~~ <u>a single input signal for generating both the PMOS output signal and NMOS output</u> signal;

changing an input signal to the multiplexer pre-driver from a first state to a second state; and

during the changing input signal, operating the multiplexer pre-driver such that both the PMOS output signal and the NMOS output signal are in a tri-state condition simultaneously.

12. (Original) The method according to claim 11, wherein during the changing input signal, operating the multiplexer pre-driver further causes the PMOS output signal and the NMOS output signal to reach their final states at different points in time.

13. (Currently Amended) A power efficiency control (PEC) circuit comprising:

a first multiplexer circuit operational to generate an upper output (UOP) pre-driver signal in response to only an input signal; and

a second multiplexer circuit operational to generate a lower output (LOP) pre-driver signal in response to only the input signal, wherein <u>the input signal is a single input signal for generating both the UOP and LOP pre-driver signals and</u> the first and second multiplexers are configured such that the UOP pre-driver signal and the LOP pre-driver signal reach their final states at different points in time in response to an input signal transition wherein the first and second multiplexers are further configured such that the

UOP pre-driver signal and the LOP pre-driver signal are simultaneously tri-stated during the input signal transition.

14. (Cancelled)

15. (Original) The PEC circuit according to claim 13, wherein the UOP pre-driver signal is a PMOS signal.

16. (Original) The PEC circuit according to claim 13, wherein the LOP pre-driver signal is an NMOS signal.